PCIe Advanced Error Reporting Plugin

Metrics List & Descriptions:

Technology /Category	Metric /Feature /Input	Name	Date Type	Format Example	Collectd Release	Collctd Plugin	Description	Dependencies	Limitations	Comments
PCIE AER		PCIe AER Plugin	-	-	-	-	Plugin to provide PCIe AER metrics, errors, notifications & device information	Depends on sysfs and proc file systems	To be used on little endian systems.	
PCIe AER	Feature	Device Domain	Hex	10	Master	pcie_errors	The PCI address domain consisting of three distinct address spaces: configuration, memory, and I/O space.	None		
PCIe AER	Feature	Device Bus	Hex	10	Master	pcie_errors	PCIe Bus number	None		
PCIe AER	Feature	Device ID	Hex	3597	Master	pcie_errors	PCIe Device ID of the device	None		
PCIe AER	Feature	Device Function	Hex	10	Master	pcie_errors	Bus:Device.Function notation used to succinctly describe PCI and PCIe devices	None		
PCIe AER	Feature	Instance Type	Text	correctable /uncorrectable	Master	pcie_errors	PCIe instance type	None		
PCIe AER	Feature	Severity	Text	Fatal /Non-fatal	Master	pcie_errors	Severity flag indicating nature of severity of uncorrectable errors with fatal or non-fatal error types	None		
PCIe AER	Feature	Persistent Notification	Text	True /False	Master	pcie_errors	If any uncorrectible error is already reported once, persistent flag is set in the plugin and not reported again	None		
PCIE AER	Metric	Uncorrectable Error	Text	uncorrectable	Master	pcie_errors	The errors which don't have impact on integrity of the PCI Express fabric, but data/information is lost. Non-fatal errors are corrupted transactions that can't be corrected by PCIe hardware. However, the PCI Express fabric continues to function correctly and other transactions are unaffected, only particular transaction is affected. Recovery from a non-fatal error may or may not, depends on device-specific software associated with the requester that initiated the transaction	None		
PCIe AER	Metric	Correctable Error	Text	correctable	Master	pcie_errors	the errors which may have an impact on performance (like latency, bandwidth), but no data/information is lost and PCIe fabric remains reliable. Such errors are corrected by hardware and no software intervention is required	None		
PCIe AER	Metric	Severity Non-Fatal Error	Text	non_fatal	Master	pcie_errors	Error severity indicating no reboot necessary	None		
PCIe AER	Metric	Severity Fatal Error	Text	fatal	Master	pcie_errors	Error severity indicating reboot necessary	None		
PCIe AER	Metric	Unsupported Request	Text	unsupported	Master	pcie_errors	This error occurs when an endpoint or a root port recieves any of a set of transactions as defined by PCIe Spec defined in [1]. In all cases the TLP is deleted in the Hard IP block and not presented to the Application Layer. If the TLP is a non-posted request, the Hard IP block generates a completion with Unsupported Request status.	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Data Link Protocol Uncorrected Error	Text	Data Link Protocol	Master	pcie_errors	This error occurs when a sequence number specified by the Ack/Nak block in the Data Link Layer (AckNak_Seq_Num) does not correspond to an unacknowledged TLP.	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Surprise Down Uncorrected Error	Text	Surprise Down	Master	pcie_errors	When the PCIe device goes down without a notice	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Poisoned TLP Uncorrected Error	Text	Poisoned TLP	Master	pcie_errors	anytime a poisoned TLP is destined to PCIe device, IIO module will drop the poisoned data packet, contain the error in the domain that it was detected in, bring down the link, and signal a fatal error to SW /FW	Depends on what's exposed in sysfs and proc file systems		

PCIe AER	Metric	Flow Control Protocol Uncorrected Error	Text	Flow Control Protocol	Master	pcie_errors	An uncorrected error in flow control protocol found in transaction layer that prevents flow control credits transactions being sent. This error occurs when a component does not receive update flow control credits with the 200 µs limit.	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Completion Timeout Uncorrected Error	Text	Completion Timeout	Master	pcie_errors	This error occurs when a request originating from the Application Layer does not generate a corresponding completion TLP within the established time. It is the responsibility of the Application Layer logic to provide the completion timeout mechanism. The completion timeout should be reported from the Transaction Layer using the cpl_err[0] signal.	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Completer Abort Uncorrected Error	Text	Completer Abort	Master	pcie_errors	The Application Layer reports this error using thecpl_err[2]signal when it aborts receipt of a TLP.	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Unexpected Completion Uncorrected Error	Text	Unexpected Completion	Master	pcie_errors	This error is caused by an unexpected completion transaction as listed in [1]. The TLP is not presented to the Application Layer; the Hard IP block deletes it.	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Receiver Overflow Uncorrected Error	Text	Receiver Overflow	Master	pcie_errors	This error occurs when a component receives a TLP that violates the FC credits allocated for this type of TLP. In all cases the hard IP block deletes the TLP and it is not presented to the Application Layer.	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Malformed TLP Uncorrected Error	Text	Malformed TLP	Master	pcie_errors	This error is caused by an unexpected completion transaction as listed in [1]. The TLP is not presented to the Application Layer; the Hard IP block deletes it.	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	ECRC Uncorrected Error Status	Text	ECRC	Master	pcie_errors	ECRC ensures end-to-end data integrity for systems that require high reliability. When the ECRC generation option is turned on, errors are detected when receiving TLPs with a bad ECRC. More details in [2]	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Unsupported Uncorrected Error Request	Text	Unsupported	Master	pcie_errors	This error is caused by an unexpected completion transaction as listed in [1]. The TLP is not presented to the Application Layer; the Hard IP block deletes it.	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	ACS Violation Uncorected Error	Text	ACS Violation	Master	pcie_errors	Violation in Access Control Services. More details in [3]	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Internal Uncorrected Error	Text	Internal Uncorrected	Master	pcie_errors	An error associated with a PCI Express interface that occurs within a component and which may not be attributable to a packet or event on the PCI Express interface itself or on behalf of transactions initiated on PCI Express. More details in [4]	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	MC Blocked TLP Uncorrected Error	Text	MC Blocked TLP	Master	pcie_errors	An error with Multicast TLP processing. More details in [5]	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Atomic Egress Blocked Uncorrected Error	Text	Atomic Egress Blocked	Master	pcie_errors	Error with setting AtomicOp Egress Blocking bit. More details in [6]	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	TLP Prefix Blocked Uncorrected Error	Text	TLP Prefix Blocked	Master	pcie_errors	The TLP Prefix mechanism extends the header size by adding DWORDS to the front of headers that carry additional information. The uncorrected error reflects failure in the process. More details in [7]	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Receiver Error Status Corrected Error	Text	Receiver Error Status	Master	pcie_errors	Receiver error at PCIe physical layer	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Bad TLP Status Corrected Error	Text	Bad TLP Status	Master	pcie_errors	This error occurs when a LCRC verification fails or when a sequence number error occurs.	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Bad DLLP Status Corrected Error	Text	Bad DLLP Status	Master	pcie_errors	This error occurs when a CRC verification fails.	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Replay NUM Rollover Corrected Error	Text	Replay NUM Rollover	Master	pcie_errors	This error occurs when the replay number rolls over.	Depends on what's exposed in sysfs and proc file systems		

PCIe AER	Metric	Replay Timer Timeout Corrected Error	Text	Replay Timer Timeout	Master	pcie_errors	This error occurs when the replay timer times out	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Advisory Non-Fatal Corrected Error	Text	Advisory Non-Fatal	Master	pcie_errors	The error are reported and signaled as ERR_COR, ERR_NONFATAL, ERR_FATAL or not signaled at all, depending upon the role of the agent that detects the error and whether the agent implements AER as an advisory capacity to application. More details in [8]	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Corrected Internal Corrected Error	Text	Corrected Internal	Master	pcie_errors	An error associated with a PCI Express interface that occurs within a component and which may not be attributable to a packet or event on the PCI Express interface itself or on behalf of transactions initiated on PCI Express. More details in [4]	Depends on what's exposed in sysfs and proc file systems		
PCIe AER	Metric	Header Log Overflow Corrected Error	Text	Header Log Overflow	Master	pcie_errors	When a header is logged, the header is that of the first TLP that was lost or corrupted by the Uncorrectable Internal Error. More detilas in [9]	Depends on what's exposed in sysfs and proc file systems		

Sub-sections:

PCIe Errors High Level Design

PCIe RAS Executed Tests