

PMU

Metrics List & Dependencies:

T e c h n o l o g y / C a t e g o r y	M e t r i c / F e a t u r e / I n p u t	N a m e	D a t e T y p e	Format Example	C o l l e c t e d R e l e a s e	C o l l e c t e d P l u g i n	Description	D e p e n d e n c i e s	Limitations	B a r o m e t e r V e r i f i e d (Y e s / N o)	Comments
P M U	M e t r i c	L1-dcache - loads	I n t e g e r	23734	5.8	i n t e l _ p m u	Level 1 cache for data (L1d) read accesses by a CPU core	j e v e n t s f r o m p m u - t o o l s		yes	Dependent on jevents library to read the metric value
P M U	M e t r i c	L1-dcache - load - misses	I n t e g e r	23734	5.8	i n t e l _ p m u	Level 1 cache for data (L1d) read misses by a CPU core	j e v e n t s f r o m p m u - t o o l s		yes	Dependent on jevents library to read the metric value
P M U	M e t r i c	L1-dcache - stores	I n t e g e r	23734	5.8	i n t e l _ p m u	Level 1 cache for data (L1d) writes by a CPU core	j e v e n t s f r o m p m u - t o o l s		yes	Dependent on jevents library to read the metric value
P M U	M e t r i c	L1-dcache - store - misses	I n t e g e r	23734	5.8	i n t e l _ p m u	Level 1 cache for data (L1d) write misses by a CPU core	j e v e n t s f r o m p m u - t o o l s		yes	Dependent on jevents library to read the metric value
P M U	M e t r i c	L1-dcache - prefetches	I n t e g e r	23734	5.8	i n t e l _ p m u	Level 1 cache for data (L1d) prefetch accesses by a CPU core	j e v e n t s f r o m p m u - t o o l s		yes	Dependent on jevents library to read the metric value
P M U	M e t r i c	L1-dcache - prefetch - misses	I n t e g e r	23734	5.8	i n t e l _ p m u	Level 1 cache for data (L1d) prefetch misses by a CPU core	j e v e n t s f r o m p m u - t o o l s		yes	Dependent on jevents library to read the metric value

P MU	M etric	L1- icac- he- loads	Int eger	23734	5.8	in te l_ p mu	Level 1 cache for instructions (L1i) read accesses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	L1- icac- he- load - mis ses	Int eger	23734	5.8	in te l_ p mu	Level 1 cache for instructions (L1i) read misses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	L1- icac- he- pref etch es	Int eger	23734	5.8	in te l_ p mu	Level 1 cache for instructions (L1i) prefetch accesses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	L1- icac- he- pref etch - mis ses	Int eger	23734	5.8	in te l_ p mu	Level 1 cache for instructions (L1i) prefetch misses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	LLC - loads	Int eger	23734	5.8	in te l_ p mu	Last level cache (LLC) read accesses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	LLC - load - mis ses	Int eger	23734	5.8	in te l_ p mu	Last level cache (LLC) read misses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	LLC - stor es	Int eger	23734	5.8	in te l_ p mu	Last level cache (LLC) writes by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	LLC - stor e- mis ses	Int eger	23734	5.8	in te l_ p mu	Last level cache (LLC) write misses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value

P MU	M etric	LLC - prefetches	Integer	23734	5.8	in te l_ p mu	Last level cache (LLC) prefetch accesses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	LLC - prefetch - misses	Integer	23734	5.8	in te l_ p mu	Last level cache (LLC) prefetch misses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	dTL B- loads	Integer	23734	5.8	in te l_ p mu	Translation lookaside buffer for data (dTLB) read accesses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	dTL B- load - misses	Integer	23734	5.8	in te l_ p mu	Translation lookaside buffer for data (dTLB) read misses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	dTL B- stores	Integer	23734	5.8	in te l_ p mu	Translation lookaside buffer for data (dTLB) writes by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	dTL B- store- misses	Integer	23734	5.8	in te l_ p mu	Translation lookaside buffer for data (dTLB) write misses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	dTL B- prefetches	Integer	23734	5.8	in te l_ p mu	Translation lookaside buffer for data (dTLB) prefetch accesses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	dTL B- prefetch - misses	Integer	23734	5.8	in te l_ p mu	Translation lookaside buffer for data (dTLB) prefetch misses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value

P MU	M etric	iTL B- loads	Int eger	23734	5.8	in te l_ p mu	Translation lookaside buffer for instructions (iTLB) read accesses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	iTL B- load - mis ses	Int eger	23734	5.8	in te l_ p mu	Translation lookaside buffer for instructions (iTLB) read misses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	bran ch - loads	Int eger	23734	5.8	in te l_ p mu	Branch prediction unit read accesses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	bran ch - load - mis ses	Int eger	23734	5.8	in te l_ p mu	Branch prediction unit read misses by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	cpu - cycl es	Int eger	23734	5.8	in te l_ p mu	Total CPU cycles by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	instr ucti ons	Int eger	23734	5.8	in te l_ p mu	Retired instructions by a CPU core	je ve nt s fro m p m u- to ols	Note: these can be affected by various issues, most notably hardware interrupt counts.	yes	Dependent on jevents library to read the metric value
P MU	M etric	cac he- refe ren ces	Int eger	23734	5.8	in te l_ p mu	Cache accesses per CPU core. Usually this indicates Last Level Cache accesses but this may vary depending on CPU type.	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	cac he- mis ses	Int eger	23734	5.8	in te l_ p mu	Cache read misses by a CPU core. Usually this indicates Last Level Cache misses.	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value

P MU	M etric	branch es	Integer	23734	5.8	in te l_ p mu	Retired branch instructions by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	branch - mis ses	Integer	23734	5.8	in te l_ p mu	Mispredicted branch instructions by a CPU core	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	bus - cycl es	Integer	23734	5.8	in te l_ p mu	Bus cycles per CPU core, which can be different from total cycles.	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	cpu - clock	Integer	23734	5.8	in te l_ p mu	Reports the CPU clock, a high-resolution per-CPU timer, by a CPU core. Software event provided by the kernel.	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	task - clock	Integer	23734	5.8	in te l_ p mu	Reports a clock count specific to the task that is running, by a CPU core. Software event provided by the kernel.	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	cont ext- swit ches	Integer	23734	5.8	in te l_ p mu	Number of context switches per CPU core. Software event provided by the kernel.	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	cpu - mig rati ons	Integer	23734	5.8	in te l_ p mu	Number of times the process has migrated to a new CPU, by a CPU core. Software event provided by the kernel.	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	pag e- faults	Integer	23734	5.8	in te l_ p mu	Number of page faults by a CPU core. Software event provided by the kernel.	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value

P MU	M etric	min or- faults	Int eger	23734	5.8	in te l_ p mu	Number of minor page faults by a CPU core. Software event provided by the kernel.	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	maj or- faults	Int eger	23734	5.8	in te l_ p mu	Number of major page faults by a CPU core. Software event provided by the kernel.	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	alig nment- faults	Int eger	23734	5.8	in te l_ p mu	Number of alignment faults by a CPU core. These happen when unaligned memory accesses happen. Software event provided by the kernel.	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	M etric	emulati on- faults	Int eger	23734	5.8	in te l_ p mu	Number of emulation faults by a CPU core. The kernel sometimes traps on unimplemented instructions and emulates them for user space. Software event provided by the kernel.	je ve nt s fro m p m u- to ols		yes	Dependent on jevents library to read the metric value
P MU	In put	Cor es	Int eger Ar ray as St ring	"[0-12]" or "1,2,3"	5.8.1	in te l_ p mu	The list of CPU core(s) to be provided as input by the user for which the corresponding metrics are required	N one	None		Configuration input in the plugin .conf file
P MU	In put	Con figu ration Inte rval	Int eger	1 or 10	5.8	in te l_ p mu	The interval in seconds at which the metrics need to be collectd	N one	None		Configuration input in the plugin .conf file
P MU	In put	Rep ort Har dwa re Cac he Eve nts	B oole an	true/false	5.8	in te l_ p mu	Report hardware CPU cache events, list in comments	N one	None		L1-dcache-loads, L1-dcache-load-misses, L1-dcache-stores, L1-dcache-store-misses, L1-dcache-prefetches, L1-dcache-prefetch-misses, L1-icache-loads, L1-icache-load-misses, L1-icache-prefetches, L1-icache-prefetch-misses, LLC-loads, LLC-load-misses, LLC-stores, LLC-store-misses, LLC-prefetches, LLC-prefetch-misses, dTLB-loads, dTLB-load-misses, dTLB-stores, dTLB-store-misses, dTLB-prefetches, dTLB-prefetch-misses, iTLB-loads, iTLB-load-misses, branch-loads, branch-load-misses
P MU	In put	Rep ort Ker nel PM U Eve nts	B oole an	true/false	5.8	in te l_ p mu	Report generalized hardware CPU events. Not all of these are available on all platforms. List in comments.	N one	None		cpu-cycles, instructions, cache-references, cache-misses, branches, branch-misses, bus-cycles
P MU	In put	Rep ort Soft war e Eve nts	B oole an	true/false	5.8	in te l_ p mu	Software events provided by the kernel. List in comments.	N one	None		cpu-clock, task-clock, context-switches, cpu-migrations, page-faults, minor-faults, major-faults, alignment-faults, emulation-faults
P MU	In put	Eve nt List	St ring	"pmu- events /Genuine Intel-6- 55-core. json"	5.8	in te l_ p mu	Path to file with custom hardware events. The should containt description and definition for events available for given CPU type.	N one	File should be valid for supported CPU type.		Valid file for current CPU type can be obtained with use of event_download tool: https://raw.githubusercontent.com/andikleen/pmu-tools/master/event_download.py

P MU	In p ut	Har dwa re Eve nts	St rin g Ar ray	L2_RQS TS. CODE_ RD_HIT, L2_RQS TS. CODE_ RD_MISS	5.8	in te l_ p mu	Custom hardware events for given CPU type. Names of events must be available in "Event List" json file.	ev en t_ do w nl oa d. py to ol	No		If there are more events than counters, the kernel uses time multiplexing. With multiplexing, at the end of the run, the counter is scaled basing on total time enabled vs time running.
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Sub-sections:

[PMU plugin High Level Design](#)

[Intel PMU Executed Tests](#)

[Intel PMU Performance considerations](#)